IN THE SPECIFICATION:

Applicant submits as a new paragraph and a new phrase and replacement phrases to address the addition of new Figure 8. Applicant submits that no new matter is injected into the application by way of the substitute paragraphs.

Please replace the phrase beginning at page 4, line 22, with the following phrase:

Fig. 6 shows a schematic of the overall design of a processor with pipelined architecture for the purpose of executing conditional jump instructions with the branch prediction according to the invention; ~~and~~

Please replace the phrase beginning at page 4, line 27, with the following phrase:

Fig. 7 shows a detailed illustration of a processor with apparatuses for the branch prediction according to the invention[.]; and

Please insert the following new phrase beginning at page 4, line 31, after the phrase beginning with "Fig. 7 shows . . .":

Fig. 8 shows a simple flowchart illustrating a method for processing conditional jump instructions in a processor with pipeline computer architecture.

Please insert the following new paragraph beginning at page 17, line 22, after the paragraph beginning with "It is possible in this way according to the invention. . .":

Figure 8 shows a simple flowchart of a method 110 for processing conditional jump instructions in a processor with pipeline computer architecture. The method

includes loading and decoding a processor instruction as shown in block 112. The processor instruction can contain an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. The precondition comprises at least one precondition bit that specifies under which conditions the instruction is actually to be executed. The post-condition specifies that a conditional jump is to be processed and that the corresponding flag bits of an arithmetic-logic unit are to be checked, wherein the post-condition comprises at least one post-condition bit that is checked in the processor. The method also includes checking the precondition as shown in block 114, and executing the decoded processor instruction if the precondition is fulfilled as shown in block 116. In the case of a fulfilled precondition, the post-condition is checked as shown in block 118. No jump is carried out if the post-condition is not fulfilled as shown in block 120, and the corresponding flag bits are checked if the post-condition is fulfilled as shown in blocks 122 and 124. The method further includes jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set as shown in block 126. This method and its associated steps are explained in detail above.